30. (amended) An integrated circuit device comprising:

input receiver circuitry to sample an operation code synchronously with respect to a first transition of an external clock signal;

output driver circuitry to output data in response to the operation code specifying a read operation, wherein:

the output driver circuitry outputs a first portion of data in response to a rising edge transition of the external clock signal; and

the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal.

31. The integrated circuit device of claim 30 further including a memory array having a plurality of memory cells.

32. The integrated circuit device of claim 31 wherein the input receiver circuitry receives address information synchronously with respect to the external clock signal.

33. (amended) The integrated circuit device of claim 32 wherein the input receiver circuitry samples the address information synchronously with respect to a second transition of the external clock signal.

34. The integrated circuit device of claim 32 wherein the operation code and the address information are included in a packet.

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35 ~~185~~. The integrated circuit device of claim 30 ~~180~~ further including a clock alignment circuit to receive the external clock signal.

36 ~~186~~. The integrated circuit device of claim 35 ~~185~~ wherein the clock alignment circuit generates an internal clock signal, and the output driver circuitry outputs data in response to the internal clock signal.

37 ~~187~~. (amended) The integrated circuit device of claim 30 ~~180~~ wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

38 ~~188~~. (amended) The integrated circuit device of claim 30 ~~180~~ wherein the rising edge transition of the external clock signal and the falling edge transition of the external clock signal transpire in one clock cycle of the external clock signal.

39 ~~189~~. The integrated circuit device of claim 30 ~~180~~ wherein the input receiver circuitry receives block size information synchronously with respect to the external clock signal, wherein the block size information indicates an amount of data to be output by the output driver circuitry.

40 ~~190~~. (amended) The integrated circuit device of claim 30 ~~180~~ wherein the input receiver circuitry receives a value which is representative of a number of clock cycles of the external clock signal to transpire before the output driver circuitry outputs data.

41 ~~101~~. (amended) The integrated circuit device of claim 40 ~~100~~ further including a programmable register to store the value which is representative of a number of clock cycles of the external clock signal to transpire before the output driver circuitry outputs data.

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